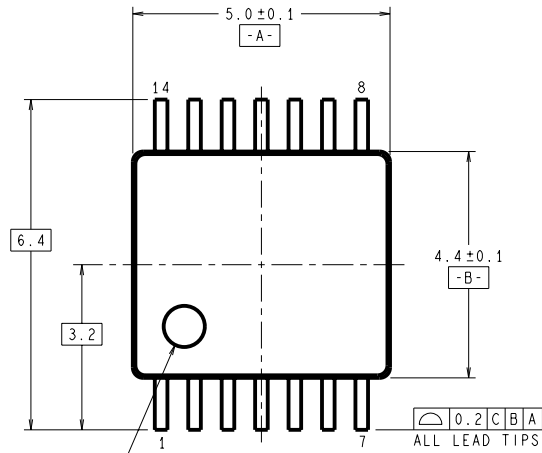
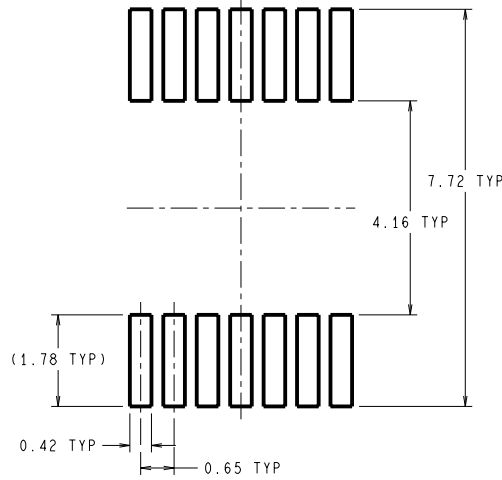


REVISIONS

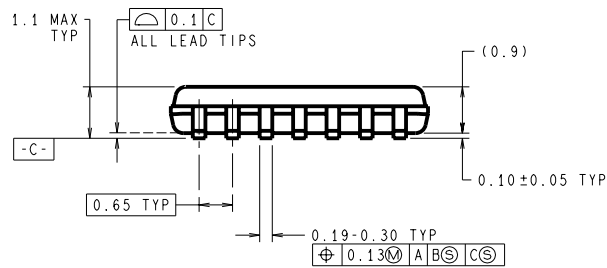
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
C	REVISE & REDRAW ON PRO/E PER CURRENT STD; CORRECT DET CALLOUT FROM D TO A.	11099	08/21/95	MS/



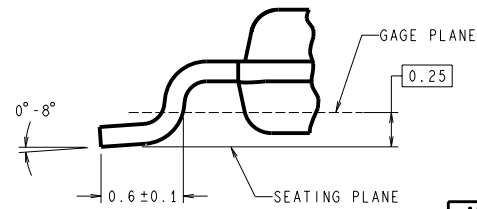
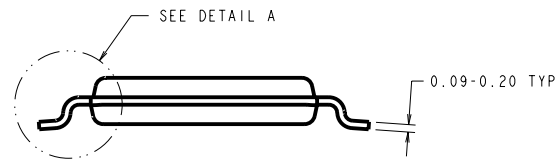
PIN #1 IDENT.



LAND PATTERN RECOMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A  
TYPICAL, SCALE: 40X

NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93.

APPROVALS		DATE	National Semiconductor			
DRAWN	MARTA SUCHY	08/21/95	2900 Semiconductor dr., Santa Clara, CA 95052-8090			
DFTG. CHK.			<b>MOLDED TSSOP, JEDEC, 4.4mm BODY WIDTH, 14 LD, 0.65mm PITCH</b>			
ENGR. CHK.						
PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV	
		N/A	C	MKT-MTC14	C	
DO NOT SCALE DRAWING			SHEET 1 of 1			